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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,611	09/12/2003	Chun Ho Fan	50626.55	6110

35510 7590 05/26/2005

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 05/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,611	FAN ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *1-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/8/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicants' election without traverse of Group II, i.e., Claims 11-25, in the reply filed on April 29, 2005 is acknowledged.

2. Accordingly, claims 1-12 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on April 29, 2005.

Drawings

3. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 15 objected to because of the following informalities:

Claim 15 recites the limitation "substrate" in line 2.

The examiner respectfully suggests changing "substrate" to --said substrate-- in order to maintain proper antecedent bases and consistency. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 13-17, 20-22, 24 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al. (US/2002/0113308).

Re claim 13, Huang et al. disclose an integrated circuit package comprising: a substrate (20) having a plurality of conductive traces (22) (i.e., i.e., plurality of gold wires **22** which commonly known as **a conductive trace** in the art) (see Fig. 1); a plurality of balls (230) (i.e., the solder balls **230**) disposed on a first surface of the substrate (20) (see Fig. 1); a semiconductor die (21) (i.e., the semiconductor chip **21** and also known as semiconductor die) mounted to the substrate (20) such that bumps (230) of the semiconductor die (21) are electrically connected to conductive traces of the substrate (see Fig. 1); an overmold material encapsulating (25) (i.e., encapsulant **25**) the semiconductor die (21) and the balls (230) on the substrate such that portions of the balls are exposed (see Fig. 1); and a ball grid array (24) in electrical connection with the conductive traces (See Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]).

Re claim 14, as applied to claim 13 above, Huang et al. disclose all the claimed limitations including the limitation wherein the ball grid array (24) is disposed on a second surface of the substrate (20) (See Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]).

Re claim 15, as applied to claim 13 above, Huang et al. disclose all the claimed limitations including the limitation wherein the plurality of balls (230) is attached to respective solder ball pads (see Abstract) on first surface of the substrate (20) (See Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]).

Re claim 16, as applied to claim 13 above, Huang et al. disclose all the claimed limitations including the limitation wherein the bumps (i.e., the ball grid array **24**) of the semiconductor die (21) are electrically connected to the conductive traces (22) by wire bonds (See Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]).

Re claim 17, as applied to claim 13 above, Huang et al. disclose all the claimed limitations including the limitation wherein the semiconductor die is fixed to the first surface of the substrate (See Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]).

Re claim 20, as applied to claim 13 above, Huang et al. disclose all the claimed limitations including the limitation wherein the plurality of balls circumscribe the semiconductor die (See Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]).

Re claim 21, as applied to claim 13 above, Huang et al. disclose all the claimed limitations including the limitation wherein the plurality of balls electrically connected to the conductive traces of the substrate (See Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]).

Re claim 22, as applied to claim 13 above, Huang et al. disclose all the claimed limitations including the limitation wherein the balls are deformed (i.e., the solder balls 230 are

formed by reflow that requires deformation process) (See Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]).

Re claim 24, as applied to claim 13 above, Huang et al. disclose all the claimed limitations including the limitation further comprising a heat spreader (231) mounted to the balls (See Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]).

Re claim 25, as applied to claim 13 above, Huang et al. disclose all the claimed limitations including the limitation wherein the plurality of balls is comprised of a plurality of solder balls (See Figs. 1 and 5-6 and related text in Paragraphs [0023] through Paragraph [0046]).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 18 and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US/2002/0113308), as applied in Paragraph 6 above, in view of Zhao et al. (US/6,882,042).

Re claims 18 and 19, as applied to claim 13 in Paragraph 6 above, Huang et al. disclose all the claimed limitations.

However, Huang et al. do not specifically a metal strip laminated to a second surface of the substrate, wherein bumps of the ball grid array are mounted to said plurality of balls and wherein the semiconductor die is mounted to the metal strip in a cavity in the substrate such that the semiconductor die is mounted to the substrate via the metal strip.

Zhao et al. disclose a metal strip laminated to a second surface of the substrate, wherein bumps of the ball grid array are mounted to said plurality of balls and wherein the semiconductor die (114) is mounted to the metal strip in a cavity in the substrate such that the semiconductor die is mounted to the substrate via the metal strip (see Figs. 1-17 and Abstract). As Zhao et al. disclose the metal strip and the cavity provided connection with the solder balls (122) which used for the external connection.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Huang et al. '0113308 reference with a metal strip laminated to a second surface of the substrate, wherein bumps of the ball grid array are mounted to said plurality of balls and wherein the semiconductor die is mounted to the metal strip in a cavity in the substrate such that the semiconductor die is mounted to the substrate via the metal strips taught by Zhao et al. in order provide external connection solder balls.

9. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (US/2002/0113308), as applied in Paragraph 6 above, in view of Huang et al. (US/6,707,167).

Re claim 23, Huang et al. disclose all the claimed limitations except a die adapter mounted on said semiconductor die and encapsulated in the overmold material.

Huang et al. '167 disclose an IC package that a die adopter (16) that is mounted on the semiconductor die (12) which encapsulated in the overmold material (14) (see Fig. 2). As Huang et al. '167 disclose the die adopter 16 prevents cracking of the IC die (see Col. 3, lines 38-55).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Huang et al. '0113308 reference with die adopter as taught by Huang et al. '167 in order to prevent die cracking.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Wu (US/6,602,737) and Pedron, Jr. (US/6,818,980) also disclose similar inventive subject matter.

Correspondence

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede

Brook Kebede
Examiner
Art Unit 2823

BK
May 25, 2005